IEEE CTSoc Chapter MP- section: Technical Talk

4th June 2024, 6.00 PM IST

1. **Speaker name: Dr. Benjamin Carrion Schafer**

2. **Speaker Bio:** Dr. Benjamin Carrion Schafer completed his Ph.D. at the University of Birmingham, U.K. in 2003. He then worked in the Computer Science Department at the University of California Los Angeles (UCLA) as a Postdoctoral Researcher from 2003 to 2004 and joined the School of Electronic Engineering and Computer Science at Seoul National University, Korea, as a Visiting Research Scholar from 2005 to 2007. From 2007 until September 2012, he was a researcher at the System IP Core Department, Central R&D Centre, NEC Corporation, Kawasaki, Japan. From 2012 to 2016, he worked as an assistant professor at the Department of Electronic and Information Engineering (EIE) at the Hong Kong Polytechnic University, where he established the Design Automation and Reconfigurable Computing Laboratory (DARClab). Since 2016, he works as at the Department of Electrical and Computer Engineering at the University of Texas at Dallas where he is an associate Professor. He is the recipient of the Early Career Scheme from the Research Grants Council, Hong Kong. Dr. Carrion Schafer has been engaged in the research and development of VLSI systems, reconfigurable computing, thermal-aware VLSI design and High-Level Synthesis (HLS). He has over 30 publications as first author in international scientific journals, conferences and books. He has served on the TPC of most EDA and FPGA conferences including ASP-DAC, DATE, DAC, FPL, ICCAD and ICCD. He is the recipient of the Best Paper Award from the 2022 ACM Great Lake Symposium of VLSI (GLSVLSI'22) conference. He was also a member of Accellera's SystemC synthesizable user group committee, leading the effort to standardize a synthesizable subset of SystemC.

3. **Title of talk:** High-Level Synthesis: Adoption and Key Advantages

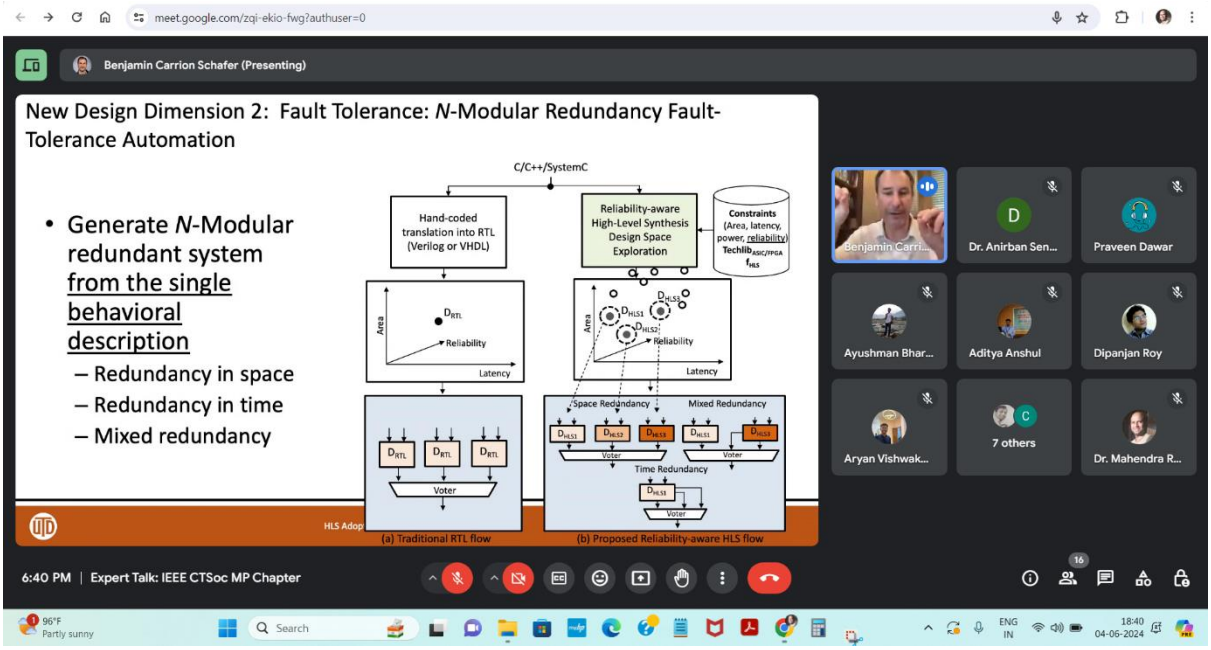
4. **Abstract of talk:** This seminar will start by explaining what High-Level synthesis (HLS) and how it works. It will continue describing some key advantages of HLS over traditional RT-level based VLSI design methodologies based on low-level hardware description languages like Verilog or VHDL. Finally, we will highlight how these advantages can be leveraged to create cheaper, safer, and more reliable hardware circuits.

5. **Date and time:** June 4th, 2024, Time: 6:00 PM IST (7.30 am CST (Dallas time))

6. **Meeting Venue:** meet.google.com/zqi-ekio-fwg

7. **Number of participants: 16**

8. Event Photo:



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