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121. Vipul Mishra, **Anirban Sengupta** "Swarm Intelligence Driven Design Space Exploration: An Integrated Framework for Power-Performance Trade-off in Architectural Synthesis", **Proceedings of 25th IEEE International Conference on Microelectronics (ICM 2013)**, Dec 2013, pp. 1 - 4.
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123. **Anirban Sengupta** "A Methodology for Self-Correction Scheme Based Fast Multi Criterion Exploration and Architectural Synthesis of Data Dominated Applications", **Proceedings of IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI-2013)**, August 2013, Mysore, pp.430 - 436.
124. **Anirban Sengupta** "An Architecture Synthesis Tool for Rapid Multi-Objective Exploration and RTL Circuit Generation", **ACM International Conference on Advances in Computing & Artificial Intelligence**, **Accepted**, 2013.
125. **Anirban Sengupta**, Reza Sedaghat, "Priority Function Driven Design Space Exploration in High Level Synthesis Based on Power Gradient Technique", **Accepted in Student Forum of 17th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC 2012)**, Australia, pp: 25, 2012.
126. **Anirban Sengupta**, Reza Sedaghat, "Integrated Scheduling, Allocation and Binding in High Level Synthesis using Multi Structure Genetic Algorithm based Design Space Exploration System", **Proceedings of 12th IEEE/ACM International Symposium on Quality Electronic Design (ISQED 2011)**, **Silicon Valley**, California, USA, March 2011, pp. 486-494 (BLIND REVIEW).
127. **Anirban Sengupta**, Reza Sedaghat, "A Hybrid Fuzzy Search Approach for Fast Design Space Exploration of Multi-Objective VLSI Systems", **Accepted in the Student Forum of 16th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC 2011)**, Japan, 2011, Paper ID: SF15.
128. **Anirban Sengupta**, Reza Sedaghat, Pallabi Sarkar, "Integrated Scheduling, Allocation and Binding in High Level Synthesis for Performance-Area Tradeoff of Digital Media Applications", **Proceedings of 24th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE 2011)**, Canada, May 2011, pp. 533-537.
129. **Anirban Sengupta**, Reza Sedaghat, Pallabi Sarkar, "Priority Function based Power Efficient Rapid Design Space Exploration of Scheduling and Module Selection in High Level Synthesis", **Proceedings of 24th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE 2011)**, Niagara, Canada, May 2011, pp. 538-543.
130. Pallabi Sarkar, Reza Sedaghat, **Anirban Sengupta**, "Power Gradient Based Design Space Exploration in High Level Synthesis for DSP Kernels", **Proceedings of 23rd IEEE International Conference on Microelectronics (ICM)**, pp: 16, December 2011.
131. **Anirban Sengupta**, Reza Sedaghat, Pallabi Sarkar "Integrated Design Space Exploration Based on Power-Performance Trade-off using Genetic Algorithm", **Proceedings of ACM International Conference on Advances in Computing and Artificial Intelligence**, 2011, pp. 76-80.
132. Pallabi Sarkar, Reza Sedaghat, **Anirban Sengupta**, "Application Specific Processor vs. Microblaze Soft Core RISC Processor: FPGA Based Performance and CPR Analysis", **Proceedings of ACM International Conference on Advances in Computing and Artificial Intelligence**, 2011, pp.81-84.
133. Summit Sehgal, Reza Sedaghat, **Anirban Sengupta**, "Automated Design Space Exploration for DSP Applications High Level Synthesis with Stability in Competition", **Accepted for Publication, Proceedings of 2nd IEEE Latin American Symposium on Circuits and Systems (LASCAS)**, Columbia, February 2011.
134. **Anirban Sengupta**, Reza Sedaghat, Zhipeng Zeng, "Rapid Design Space Exploration for multi parametric optimization of VLSI designs", **Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)**, Paris, France, pp: 3164-3167, June 2, 2010.
135. Zhipeng Zeng, Reza Sedaghat, **Anirban Sengupta**, "A Framework for Fast Design Space Exploration using Fuzzy search for VLSI Computing Architectures", **Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)**, Paris, France, 2010, pp: 3176-3179.
136. **Anirban Sengupta**, Reza Sedaghat, "Accelerated Exploration of Cost-Performance Tradeoffs for Multi Objective VLSI designs", **Proceedings of 22nd IEEE International Conference on Microelectronics (ICM)**, 2010, pp. 100-103.
137. **Anirban Sengupta**, Reza Sedaghat "Rapid Exploration of Power-Delay Tradeoffs using Hybrid Priority Factor

- and Fuzzy Search", In **Proceedings of 22nd IEEE International Conference on Microelectronics (ICM)**, Egypt,2010, pp. 355-358.
138. **Anirban Sengupta**, Reza Sedaghat, "Fast Design Space Exploration for Multi Parametric Optimized VLSI and SoC Designs", Accepted in Student Forum of **15th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC 2010)**,Taiwan, 2010,ID: 26.
139. **Anirban Sengupta**, Reza Sedaghat, "A Study on Architecture Optimization of the RISC Processor used for System-on Chip (SoC) design", In **Proceedings of Research Innovation Symposium, Ryerson University**, Canada, 2010, pp: 31.
140. Summit Sehgal, Reza Sedaghat, **Anirban Sengupta**, "Fault Monitoring Transformer Reliability ASIC Design based on Ringing Effect Signature Analyzer", **Proceedings of Research Innovation Symposium, Ryerson University**, Canada, 2010, pp: 32.
141. **Anirban Sengupta**, Reza Sedaghat, Zhipeng Zeng, "Hardware Efficient Design of speed optimized Power stringent Application Specific Processor", **Proceedings of 21st IEEE International Conference on Microelectronics (ICM)**, Morocco, pp: 167-170, December 22, 2009.
142. Summit Sehgal, Reza Sedaghat, **Anirban Sengupta**, Zhipeng Zeng, "Multi Parametric Optimized Architectural Synthesis of an Application Specific Processor", **Proceedings of 14th IEEE International CSI Computer Conference (CSICC)**,2009, pp: 89-94.
143. Zhipeng Zeng, Reza Sedaghat, **Anirban Sengupta**, "A Novel Framework of Optimizing Modular Computing Architecture for multi objective VLSI designs", **Proceedings of 21st IEEE International Conference on Microelectronics (ICM)**,Morocco, 2009, pp: 322-325.
144. **Anirban Sengupta**, Prasenjit Pal and S.K. Roy (Aug 1st & 2nd- 2008) "Problems Associated with CDMA Based Communication Systems Results and Discussions ",Accepted for poster presentation in the **IEEE and IEI, the National Conference on "Device, intelligent systems and communication& networking**, Paper No: CN_27.

IV. THESIS/DISSERTATION

145. **Anirban Sengupta**, "A Fast Design Space Exploration Based on Priority Factor for a Multi Parametric Optimized High Level Synthesis Design Flow", **Master of Applied Science (M.A.Sc) Thesis, Ryerson University, Toronto, Canada**, 2010,(**Nominated for Governor Generals Gold Medal in Canada for the Master's Thesis**). Available at Ryerson University, Toronto Library.
146. **Anirban Sengupta**, "Rapid and Efficient Multi Objective Design Space Exploration in High Level Synthesis of Computation Intensive Applications", **Doctor of Philosophy (Ph.D.) Thesis, Ryerson University, Toronto, Canada**, 2012.

IV. TECHNICAL REPORTS FOR INDUSTRY/IP OFFICE

147. **Anirban Sengupta**, Reza Sedaghat "Exploration Synthesizer: Design Automation Platform (DAP): Multi objective Design Space Exploration and Architectural Synthesis of Application kernels", No. of Pages: 14, **Organization: Ryerson University (OPRAL Research Lab), MaRS Innovation, Aventis Consulting Group Inc and Venssa Technologies**.
148. **Anirban Sengupta** "Architectural Synthesis of Digital Systems (System Level Design)" , No. of pages: 39,**Organization: Ryerson University (OPRAL Research Lab)** (Co-author: Pallabi Sarkar)
149. **Anirban Sengupta** "An ASIC Implementation Design Flow of Function Specific Processor- System Level, Logic Level and layout level Synthesis" , No. of pages: 67,**Organization: Ryerson University (OPRAL Research Lab)** (Co-author: Pallabi Sarkar)
150. **Anirban Sengupta** "Performance Analysis of FPGA based ASP vs. Embedded Microblaze RISC Processor", No. of pages: 46,**Organization: Ryerson University (OPRAL Research Lab)**, (Co-author: Pallabi Sarkar)

INDUSTRY/PATENT CITATIONS AND TECHNOLOGY TRANSFER OF MY PATENTS

1. Patent 1666/MUM/2015 – Accepted for commercialization by VividSparks IT Solutions Pvt Ltd.
2. Patent 4466/MUM/2015 – Accepted for commercialization by VividSparks IT Solutions Pvt Ltd.
3. Patent no. US 8,397,204 – Cited/used by the following industries:

Citing Patent	Filing date	Publication date	Applicant
US8826199	May 27, 2011	Sep 2, 2014	Ryerson University
US9111059	Nov 1, 2013	Aug 18, 2015	Stc. Unm
US9337845	Jun 16, 2014	May 10, 2016	International Business Machines Corporation
US9429921	Sep 17, 2012	Aug 30, 2016	Siemens Aktiengesellschaft
US9529951	May 29, 2014	Dec 27, 2016	International Business Machines Corporation
US9542198	Jul 6, 2015	Jan 10, 2017	Stc. Unm
US20120303560	May 27, 2011	Nov 29, 2012	Reza Sedaghat
US20140074306	Sep 17, 2012	Mar 13, 2014	Siemens Corporation
US20140165021	Nov 1, 2013	Jun 12, 2014	Stc.Unm

4. Patent no CA2726091 A1 – Cited by:

Citing Patent	Filing date	Publication date	Applicant
US9542518	12. March 2015	10. Jan. 2017	Qualcomm Incorporated

MAJOR AWARDS/HONOURS

Awarded "**Outstanding Associate Editor**" Award from **IEEE TCVLSI Letter Editorial Board, IEEE Computer Society** in 2017

Awarded **IEEE Distinguished Speaker** by **IEEE Consumer Electronics Society**, 2017

Editor-in-Chief, IEEE VLSI Circuits & Systems Letter (IEEE Computer Society TC-VLSI)

Awarded '**IEEE Computer Society Technical Committee on VLSI - Best Paper Award**' in IEEE International Symposium on Nanoelectronic and Information Systems 2017.

Awarded and Honored by NIT Durgapur for conducting first ever TEQIP sponsored workshop on "**Hardware Security and its Applications**"

Elevated to **IEEE Senior Member Grade**

Inducted into **Executive Committee** of **IEEE Computer Society Technical Committee on VLSI** in 2017

Awarded prestigious national award '**Sir Visvesvaraya**' **Faculty Research Fellow** (Awarded by Ministry of Electronics & IT)

Awarded '**Best Research Paper Award 2017**' by Indian Institute of Technology Indore.

Awarded '**Excellent**' ratings by expert committee of **Department of Science & Technology (DST)** based on the performance (output) in externally funded project in 2017.

Invited to join **Editorial Board as Associate Editor** of the prestigious **IEEE Transactions on Aerospace & Electronic Systems**.

Guest Editor in prestigious **IEEE Transactions on VLSI Systems** from Sep 2016

Executive Editor of prestigious **IEEE Consumer Electronics Magazine** from Aug 2016.

Associate Editor of **IEEE Access Journal** from 2016

Awarded by prestigious '**IEEE Access Journal**' on July 2016 for research contributions in advancing engineering profession.

Associate Editor of **IET Journal on Computer & Digital Technique** from Dec 2015

Associate Editor of **IEEE VLSI Circuits & Systems Letter** (IEEE Computer Society) from 2015

Editor in prestigious '**Elsevier Microelectronics Journal**' from Aug 2016.

Honorary Chief Scientist as external affiliation by **VividSparks IT Solutions Pvt Ltd** (an electronics industry) from Aug 2016.

2 Patents from IIT Indore (4466/MUM/2015 & 1666/MUM/2015) **accepted for commercialization/licensing/product** integration by **VividSparks IT Solutions Pvt Ltd**. (NDA signed).

Invited as '**Program Chair**' of 36th IEEE International Conference on Consumer Electronics (ICCE), Las Vegas on March 2017

Invited as '**Program Chair**' of **15th IEEE International Conference on Information Technology (ICIT)** on May 2016.

Invited as '**Program Chair**' of **3rd IEEE iNIS 2017** on Aug 2016.

Invited as '**Symposium Chair**' for **IEEE iNIS 2016**.

Awarded **Ontario Graduate Scholarship (OGS)** of \$15,000 for 2012/2013 by Ministry (Provincial Level).

Awarded **Ontario Center of Excellence (OCE)** award of \$10,000 for Research (independent fund) by OPR-AL, Ryerson University, 2012.

Awarded **Graduate Research Excellence Award** of \$2,500 in PhD category at Ryerson University for 2011.

Awarded **Ontario Graduate Scholarship (OGS)** of \$15,000 for 2011/2012 by Ministry (Provincial Level).

Awarded **Graduate Research Excellence Award** of \$2,500 as **Rank # 1** in PhD category at Ryerson University for 2010

Awarded **Ontario Graduate Scholarship (OGS)** of \$15,000 for 2010/2011 by Ministry (Provincial Level).

Nominated for 2010 **NSERC Innovation Challenge Award (ICA)** by OVPRI, Ryerson University.

Awarded **Ontario Graduate Scholarship (OGS)** of \$15,000 for 2009/2010 by Ministry (Provincial Level)

Nominated for **Governor General's Gold Medal for the M.A.Sc Thesis** by the Committee at Ryerson University.

Awarded **Ryerson Graduate Award (RGA)** for \$3000 - 2008 by department of Electrical and Computer Engineering.

Awarded **RGA Electrical Engineering award** for \$1000 by Electrical and Computer Engineering, Ryerson University - 2009.

NEWS/MEDIA/PRESS COVERAGE OF MY PROFESSIONAL WORK

- “IEEE global meet on Nano-electronic and Information Systems begins”, **CENTRAL CHRONICLE**, 19th December 2017.
- “Country Needs to Focus on Research”, **THE TIMES OF INDIA**, 21st December 2017.
- “IET member receives Distinguished Lecturer accolade”, **IET INTERNATIONAL NEWS**, Nov 9, 2017
- “3rd International Meet on Info System Ends”, **THE FREE PRESS JOURNAL**, 21st December 2017.
- “IEEE-iNIS Begins”, **THE FREE PRESS JOURNAL**, 19th December 2017.
- “Meet on Information Systems”, **THE TIMES OF INDIA**, 14th December 2017.
- “3rd IEEE-iNIS 2017 to Begin”, **THE FREE PRESS JOURNAL**, 9th December 2017.
- “International Seminar for City's Scientists”, **DBPOST NEWS**, 6th December 2017.
- “IIT-Indore teacher gets intl recognition”, **THE FREE PRESS JOURNAL**, Aug 18, 2015