Design Space Explorer for High-Level-Synthesis of Digital Circuits

A **MaRS Innovation** Technology

Quick Facts

Sector:
Electronic Design Automation – High Level Synthesis

Product:
New Tool for extremely fast electronic architecture optimization against multiple simultaneous objectives

Market Size:
More than 100 Million US$ per year

Development Stage:
Web-based demonstration version of software is now available. Supports input in DFG format. Input of C, C++, and SystemC, is under development. Early testing underway with selected end-users.

Mars Innovation Project Team Member: David Asgeirsson

Inventors:
Anirban Sengupta, Reza Sedaghat

Industries interacted and demonstrated for Technological refinement

Calypto, Bluespec, BEECube, Huawei Canada

MaRS Innovation Technology and Ryerson University, Toronto, Canada

Seed Funding:
$55k from MaRS Innovation (and Ontario Center of Excellence) for development of the Demonstration Software platform

Future Plan:
Currently seeking established EDA companies for partnerships

MaRS Innovation

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Technology Profile

The Problem: Moore's Law says that the numbers of transistors in a given size of integrated circuit will double every 18 months. This exponential growth in computing power poses an enormous challenge for the engineer to quickly and reliably design, simulate, test, debug and refine new microchips. Modern electronic design automation (EDA) software allows designers to work at higher levels of abstraction, and automates many tasks. High-Level-Synthesis (HLS) tools allow the designer to describe a digital circuit in a traditional programming language like C, C++ or SystemC, and automatically generate a register-level description of the circuit. Current HLS tools are only able to optimize the architecture for one or two performance criteria, while the design engineer still has to worry about, and manually explore many tradeoffs like: chip area, power consumption, execution speed, cost, thermal load, etc.

The Technological Solution: Anirban Sengupta and Reza Sedaghat have developed the Design Space Explorer, the first HLS tool that can automatically optimize the architecture for multiple criteria simultaneously, without suffering in circuit performance.

The incredibly fast design space exploration takes place in a fraction of a second, and can deliver system architectures **simultaneously optimized** for power, speed, area, cost, and thermal behavior. Synthesis of the optimized architecture then provides an RTL or VHDL description of the circuit that is ready for use with any of the standard implementation tools for FPGA platforms or ASIC design.

This software can save the designer time, money and effort in the difficult early stage of design space exploration, to provide improved quality, and shorten the design cycle in today's competitive environment.

The Technology Developed: A beta version of the Design Space Explorer is developed which is underwent refinement based on the feedback collected from selected HLS users (industries such as Calypto, Bluespec). We are looking for partnership opportunities with some EDA tool companies in the near future.

INTELLECTUAL PROPERTY

- Anirban Sengupta, Reza Sedaghat "System and Method for Development of a System Architecture", **US Patent** 20120159119 and 13/118,139, **Canadian Patent** CA 2726091 and CA 2741253.

RESEARCH TEAM

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